

Form PTO-1449	U.S. DEPT. OF COMMERCE Patent and Trademark Office	Atty. Docket No.: 2102397-992011	Serial No.: Not yet assigned 107776,397
INFORMATION DISCLOSURE CITATION (Use several sheets if necessary)		Applicant: Kianian et al.	
		Filing Date: February 10, 2004	Group Art Unit: Not yet assigned 2822

U.S. PATENT DOCUMENTS

Examiners Initials	Patent Number	Date	Name	Class	Subclass	Filing Date
JmJ	2003/0073275	04/2003	Kianian et al.	438	201	
	4,757,360	07/12/88	Farone	257	317	
	4,794,565	12/27/88	Wu et al.	365	185.15	
	4,882,707	11/21/89	Mizutani	365	185.12	
	4,905,062	02/1990	Esquivel et al	257	316	
	4,931,847	06/05/90	Corda	365	185.28	
	4,947,221	08/07/90	Stewart et al.	257	316	
	5,021,848	06/04/91	Chiu	257	317	
	5,029,130	07/02/91	Yeh	365	185.31	
	5,041,886	08/20/91	Lee	257	320	
	5,049,515	09/1991	Tzeng	438	259	
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	5,268,319	12/07/93	Harari	438	260	
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	5,572,054	11/05/96	Wang et al.	257	322	
	5,780,341	07/14/98	Ogura	438	259	
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Examiner: T. M. Thomas	Date Considered: 06-24-05
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Form PTO-1449 U.S. DEPT. OF COMMERCE Patent and Trademark Office INFORMATION DISCLOSURE CITATION (Use several sheets if necessary)	Atty. Docket No.: 2102397-992012	Serial No.: Not yet assigned 107 776, 397
	Applicant: Kianian et al.	
	Filing Date: February 10, 2004	Group Art Unit: Not yet assigned 2022

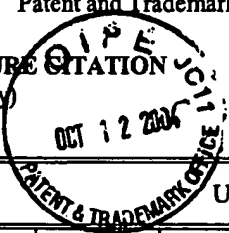
FOREIGN PATENT DOCUMENTS

	Document number	Date	Country	Class	Sub-class	Translation	
JMJ	EP 0 389 721 A2	10/03/90	Europe			YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

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		Filing date: February 10, 2004	Group art unit: 2811 2800



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Examiner Initial	Patent No. Publication No.	Date	Name	Class	Sub-class	Filing date if appropriate
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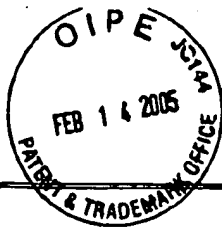
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Document number	Date	Country	Class	Sub-class	Translation YES NO

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JMJ	HAYASHI, Fumihiko and PLUMMER, James D., "A Self-Aligned Split-Gate Flash EEPROM Cell With 3-D Pillar Structure", 1999 Symposium on VLSI Technology Digest of Technical Papers, Center for Integrated System, Stanford University, Stanford, CA 94305, USA, pages 87-88
JMJ	SZE, Simon, "Physics of Semiconductor Devices", 2nd Edition, Wiley-Interscience, Basic Device Characteristics, pages 438-439.
JMJ	BROWN, William D., et al., "Nonvolatile Semiconductor Memory Technology, A Comprehensive Guide To Understanding And Using NVSM Devices", IEEE Press, pages 33-34.

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JmJ	5,998,261	12/07/99	Hofmann et al.	438	357	

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